Docket No.: M4065.0492/P492-A
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Leonard Forbes et al.

Application No.: 10/759,107 | Confirmation No.: 6955

Filed: January 20, 2004 | Art Unit: 2815

For: METHODS OF FORMING OUTPUT PREDICTION LOGIC CIRCUITS WITH ULTRA-THIN VERTICAL TRANSISTORS (AS AMENDED) | Examiner: Toniae M. Thomas

COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

While Applicants do not disagree with the Examiner's stated reasons for allowance, Applicants note that the allowed claims define unique combinations of limitations not found in the prior art. Therefore, the stated reasons for allowance should be interpreted as highlighting only some of the reasons why the claims are allowable.

As usual, the scope of the claims should be interpreted based on the actual language of the allowed claims, and no further limitation of the claims should be inferred from the Examiner's Statement of Reasons For Allowance.

Dated: November 8, 2005

Respectfully submitted,

By _____

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